Computer Architecture Fall-2019

# Assignment# 03 Marks: 100 Submission deadline: 10-1-2020

**ASSIGNMENT SHOULD BE HAND WRITTEN**

**Plagiarism policy: Do not try to copy. Students involved will be given zero straight away.**

**Question#1: [30 points]**

Consider the main memory of 64 bytes size and Cache Memory of 16 bytes. Let’s assume CPU generates following addresses: 0, 1, 2, 3, 4, 6, 7, 8, 9, 11, 16, 17, 18, 19, 20, 25, 26, 27, 28, 55, 56, 57, 58, 59, 60. Assuming cache memory **initially empty**, and **Block size: 1-byte,** Fill the **data in Cache lines** and **calculate the Hit Rate, Miss Rate,** for each of the following mapping strategies.

|  |  |
| --- | --- |
| Address | Data |
| 000000 | A0 |
| 000001 | A1 |
| 000010 | A2 |
| 000011 | A3 |
| **.** | . |
| **.** | . |
| **.** | . |
|  | . |
|  | . |
|  | . |
| 111111 | A63 |

* 1. Direct-mapped cache
  2. 2 set associative cache
  3. 4 set associative cache
  4. Fully associative cache

Table 1: **main memory 64 bytes size**

**Question#2: [30 points]**

For problem 1, find out the optimal block size which will give the maximum hit rate. Prove it by solving it for two different block size scenarios.

**Question#3: [30 points]**

For problem 1, find out which replacement policy will give maximum hit rate. Consider FIFO, LIFO, LRU and LFU as replacement policies. Calculate hit rate for each case.

**Question#4: [20 points]**

For main memory capacity of 4GB, and Cache of 8 MB, find out the number of bits in Index filed, Tag field and Byte offset fields for each of the following mapping strategies.

* 1. Direct mapping, block size 2 bytes
  2. 2- way set associative, block size 2 bytes
  3. 8 way set associative, block size 4 bytes
  4. Fully associative, block size 8 bytes